REMARKS

Reconsideration of this application, based on this amendment and these following remarks, is respectfully requested.

Claims 1 through 16 are now in this case. Claims 1 through 7 are amended. Claims 12 through 16 are added.

The Examiner objected to the drawings, on the grounds that Figure 1 and the specification were inconsistent with regard to the naming of certain elements. The specification is amended, on page 6, to correct this inconsistency; no new matter is presented by this amendment to the specification. In addition, Applicants submit that this amendment to the specification obviates the objection to the drawings, and submit that no amendment to the drawings is necessary. Accordingly, Applicants respectfully request withdrawal of the objection to the drawings.

The specification is also amended to correct the informalities noted by the Examiner, specifically by reflecting that the words "processor" and "microprocessor" are interchangeable, and by making the references to element 100 consistent throughout the specification. No new matter is presented by this amendment to the specification, and Applicants submit that this amendment obviates the objection to the specification.

Claim 1 was objected to for lacking the word "to" at a specific location. The claim is amended as suggested by the Examiner, to overcome this objection. It is submitted that this amendment to claim 1 is neither narrowing, nor presented for any reason related to patentability.[1]

[1] *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co., Ltd.*, 535 U.S. 722, 62 USPQ2d 1705 (2002), *on remand*, 304 F.3d 1289, 64 USPQ2d 1698 (Fed. Cir. 2002).

Claims 2 through 7 are amended for clarity in their preambles. Claim 7 is also amended for consistency with the antecedent basis for one of its recited limitations. The amendments to these claims are neither narrowing, nor presented for any reason related to patentability.[2]

Claims 1 and 4 were rejected under §102(b) as anticipated by the Favor et al. reference[3]. The Examiner asserted that the reference teaches all of the elements of the claims, including the execution unit (including a multiply-and-accumulate execution unit, relative to claim 4), memory interface circuitry, address pointer circuitry, and modification tracking circuitry.[4]

Applicants respectfully traverse the rejection of claims 1 and 4, on the grounds that the teachings of the Favor et al. reference fall short of the claims.

Claim 1 requires address pointer circuitry to provide an address of an operand to memory interface circuitry, and modification tracking circuitry that is operable to inhibit a redundant fetch of the operand. The Examiner specifically asserted that the Favor et al. reference teaches the modification tracking circuitry. But the locations of the Favor et al. reference cited by the Examiner do not disclose such circuitry, instead teaching that its instruction cache *causes* the fetching of an instruction from memory if the contents of the memory location of a previously fetched instruction have been modified.[5] In contrast, the modification tracking circuitry of the claimed system *inhibits* a redundant fetch of an operand (i.e., an operand that has already been fetched). Accordingly, the Favor et al. reference fails to disclose the modification tracking circuitry of claim 1, and therefore fails to anticipate claims 1 and 4 in this case. Applicants therefore respectfully traverse the §102(b) rejection of these claims.

Applicants further respectfully submit that claim 1 and its dependent claims are patentably distinct over the Favor et al. reference, considered individually or in combination with the other references applied against its dependent claims.

---

[2] *Id.*
[3] U.S. Patent No. 5,649,137, issued July 15, 1997 to Favor et al.
[4] Office Action of October 3, 2003, p. 4, ¶ 12.
[5] Fav r et al., *supra*, column 4, lines 12 through 20; column 6, lines 9 through 16.

By way of summary, claim 2 was rejected under §103 as unpatentable over the Favor et al. reference, on the additional grounds that shadow registers are known in the art, and obviously combinable with the data cache of the Favor et al. reference in order to reduce cache memory hardware and manufacturing cost.[6] Claims 3 and 7 were rejected under §103 as unpatentable over the Favor et al. reference in view of the Whitley reference[7], on the grounds that the Whitley reference teaches an indexed indirect addressing mode that corresponds to the elements of claim 3 and 7, and is obviously combined with the Favor et al. teachings.[8] Claim 5 was rejected under §103 as unpatentable over the Favor et al. reference individually, on the grounds that the one skilled in the art would have obviously implemented a cache coherency protocol with the Favor hardware,[9] and also further in view of the Schacham et al. reference[10], on the grounds that Schacham et al. teaches a cache invalidation instruction that would have been obviously combined with the Favor et al. hardware.[11] Claim 6 was rejected under §103 as unpatentable over the Favor et al. reference in view of the Okabayashi et al. reference[12], on the grounds that one skilled in the art would have obviously combined the Okabayashi et al. teachings regarding the disabling of cache circuitry during debugging with the Favor et al. teachings.[13] Claim 8 was rejected under §103 as unpatentable over the Favor et al. reference in view of the Willkie et al. reference[14]

Applicants respectfully submit that the combined teachings of the applied references fall short of the requirements of the claims, because none of the references disclose or suggest the modification tracking circuitry of claim 1. As mentioned above, the Favor et al. reference lacks teachings regarding this element. Relative to claim 2, the Examiner asserted that the knowledge of those skilled in the art includes recognition of data caches in which the cache checks for an address hit, presumably to determine whether to check access the secondary copy of data in

---

[6] Office Action, *supra*, p. 5, ¶¶ 14 through 17.
[7] U.S. Patent No. 4,531,200, issued July 23, 1985, to Whitley.
[8] Office Action, *supra*, pp. 9 and 11, ¶¶ 28 through 31.
[9] Office Action, *supra*, p. 11, ¶¶ 32 through 34.
[10] UK Patent Application Publication 2 200 481 A, published August 3, 1988.
[11] Office Action, *supra*, pp. 11 and 12, ¶¶ 32 through 36.
[12] U.S. Patent No. 6,505,309 B1, issued January 7, 2003 to Okabayashi et al.
[13] Office Action, *supra*, p
[14] U.S. Patent No. 5,923,705, issued July 13, 1999 to Willkie et al..

cache or to fetch the data from memory.[15] However, even if one accepts this as known in the art, this knowledge does not reach the requirements of claim 1 and its dependent claims, either individually or in combination with the rest of the Favor et al. reference. It is the modification tracking circuitry of claim 1 that is operable to inhibit redundant fetches of the operand. As such, the very nature of this element is that it tracks modifications, for example modifications in the contents of the address pointer circuitry; the stated function of inhibiting redundant fetches is therefore performed by this circuitry that tracks modifications. In contrast, the asserted known teachings determine which copy of data to use by comparing the desired address against those in the cache (i.e., to determine a "hit"); it is neither asserted by the Examiner nor known in the art to inhibit redundant fetches by modification tracking circuitry, as in the claimed system. Accordingly, Applicants respectfully submit that the teachings of the Favor et al. reference and the knowledge asserted by the Examiner as being in the art, properly combined, fall short of the requirements of the claims.

While the Whitley reference discloses indirect addressing of operands from memory, including indexed indirect addressing as asserted by the Examiner, it fails to teach modification tracking circuitry that inhibits redundant fetches of operands, as performed by the modification tracking circuitry of claim 1 and its dependent claims. The Schacham et al., Okabayashi et al., and Willkie et al. references similarly lack teachings in this regard, nor were they asserted as providing such teachings.

Accordingly, Applicants respectfully submit that the combined teachings of the applied references fall short of the requirements of claim 1 and its dependent claims.

Applicants further respectfully submit that there is no suggestion from the prior art to modify these combined teachings of the references to reach claim 1 and its dependent claims, considering the difference in function between the claimed system and the conventional data cache, as discussed above. The patentability of these claims is further supported by the important advantages resulting directly from the difference between the claimed digital system and the prior art. These advantages include the providing of a processor or DSP architecture in

[15] Office Action, *supra*, page 5, ¶14; *see also* Schacham et al., *supra*, page 1, lines 23 through 29.

which high code density and easy programming can be attained, particularly in minimizing coefficient fetches from memory.[16]

For these reasons, Applicants submit that amended claim 1 and its dependent claims are novel and patentably distinct over the prior art of record in this case.

New dependent claims 12 through 16 are added to more particularly recite Applicants' invention. New claim 12 further recites, relative to claim 1 upon which it depends, that the address pointer circuitry comprises a pointer register for storing at least a portion of a memory address of the operand, the contents of the pointer register being used by the memory interface circuitry to fetch operands from memory. New claim 13 further recites, relative to claim 12 upon which it depends, that the modification tracking circuitry is for detecting modifications to the memory address of an operand occurring during the execution of instructions by the execution unit, and for inhibiting a fetch of an operand responsive to the execution unit executing an instruction that uses the fetched operand and that does not modify the memory address of the operand stored in the pointer register. New claims 14 through 16 recite, relative to claims 12 or 1 upon which they depend, that the execution unit comprises one or more multiply-accumulate units.

Applicants submit that these new claims are fully supported by the specification of this application.[17] No new matter is therefore presented by new claims 12 through 16.

Applicants further respectfully submit that new claims 12 through 16 are also patentably distinct over the applied references, because the combined teachings of these references fall further short of the requirements of these claims. As mentioned above, the references wholly fail to disclose or suggest the modification tracking circuitry of claim 1. Accordingly, these references necessarily fail to disclose, and indeed fall further short of, the requirements of these new claims.

---

[16] *See* specification of S.N. 09/716,493, at page 32, line 23 through page 33, line 22.
[17] Specification, *supra*, at page 17, line 5 through page 19, line 23; page 20, line 16 through page 24, line 20.

Applicants particularly submit that the combined teachings of the references fall especially short of the requirements of new claim 13. This claim more specifically recites, relative to claim 1 upon which it indirectly depends, that the modification tracking circuitry has the functions of detecting modifications to the memory address of an operand occurring during the execution of instructions by the execution unit, and inhibiting a fetch of an operand responsive to the execution unit executing an instruction that uses the fetched operand and that does not modify the memory address of the operand stored in the pointer register (which is recited in claim 12 as storing at least a portion of a memory address of the operand). These specific recitations of claim 13 further distinguish the claimed system from the teachings of the applied references, as well as from the asserted common knowledge in the art regarding data caches and their operation.

Applicants respectfully submit that new dependent claims 12 through 16 are therefore patentably distinct over the prior art of record in this case.

Claims 9 through 11 were rejected under §103 as unpatentable over the Favor et al. reference.[18] The Examiner asserted, relative to claim 9, that the Favor et al. reference teaches all steps of the claims except for the inhibiting of fetching if the value of the data pointer has not been modified since the execution of the first instruction, but that the knowledge of those skilled in the art regarding the checking of addresses before execution against the addresses in a data cache would have been obviously combined with the Favor et al. teachings.[19] Relative to claim 10, the Examiner asserted that, while the Favor et al. reference fails to disclose the loading of a first operand into a non-accessible shadow register and, in a second instruction, not reloading this shadow register if the data pointer is not modified since execution of the first instruction, it would have been obvious to combine knowledge by the skilled artisan regarding a single entry data cache and its operation with the Favor et al. reference.[20] Regarding claim 11,

[18] Office Action, *supra*, pages 5 and 6; ¶¶ 14 through 26.
[19] Office Action, *supra*, pages 6 and 7; ¶¶ 19 and 20.
[20] Office Action, *supra*, pages 7 and 8; ¶¶ 22 and 23.

the Examiner based the rejection on the obvious combining of a known single entry data cache as a data pointer in the Favor et al. hardware.[21]

Applicants respectfully traverse the §103 rejection of claims 9 through 11 because the properly combined teachings of the applied references fall short of the requirements of claim 9. Specifically, Applicants submit that none of the references disclose or suggest the step of executing a second instruction that requires at least a second operand from memory in accordance with the data pointer (which has been loaded with a first address value), by inhibiting the fetching of that second operand from memory if the data pointer has not been modified since the step of executing the first instruction.

As mentioned above and as admitted by the Examiner, the Favor et al. reference fails to disclose this step. However, even if one accepts the assertion that one skilled in the art knows of data caches having an address pointer and data pointed to by the pointer, and the checking of an address, before execution, against addresses in the cache, this knowledge does not amount to knowledge of inhibiting fetching of a second operand if the data pointer (addressing the operand) has not been modified. The Examiner does not assert that it is known to inhibit fetching based on whether a pointer has been modified, and in fact this step (required by claim 9) is not known, is not taught by the Favor et al. reference, and is not taught by any of the other applied references. Accordingly, Applicants respectfully submit that the teachings of the Favor et al. reference and the knowledge asserted by the Examiner as being in the art, and also the other prior art of record in this case, properly combined, fall short of the requirements of claim 9 and its dependent claims.

The method of claim 9 and its dependent claims provide similar important advantages as discussed above relative to claim 1. These advantages, which include providing high code density and easy programming for a processor architecture, and improved processor efficiency by the minimizing of coefficient fetches from memory, stem directly from the difference between claim 9 and the prior art, and as such support the patentability of these claims.

---

[21] Office Action, *supra*, pages 8 and 9; ¶¶ 25 and 26.

For these reasons, Applicants respectfully submit that claims 9 through 11 are patentably distinct over the prior art of record in this case, and respectfully traverse the §103 rejection of these claims.

The prior art cited but not applied has been considered, but is not felt to come within the scope of the claims in this case.

As stated above, Applicants respectfully submit that all claims now in this case are in condition for allowance. Reconsideration of this application is therefore respectfully requested.

Respectfully submitted,

/

Rodney M. Anderson
Registry No. 31,939
Attorney for Applicants

Anderson, Levine & Lintel, L.L.P.
14785 Preston Road, Suite 650
Dallas, Texas 75254
(972) 664-9554

CERTIFICATE OF FACSIMILE TRANSMISSION
37 C.F.R. 1.8

The undersigned hereby certifies that this correspondence is being facsimile transmitted to the Patent and Trademark Office (Fax Number 703-872-9306) on February 3, 2004.

/

Rodney M. Anderson
Registry No. 31,939